WHAT IS CLAIMED IS:

1. A packet switch for switching cells comprising fixed-size data packets, said packet switch comprising:

N input ports capable of receiving and storing cells in a plurality of input queues;

N output ports capable of receiving and storing cells from said N input ports in a plurality of output queues;

a switch fabric for transferring said cells from said N input ports to said N output ports, said switch fabric comprising an internally buffered crossbar having NxN internal buffers associated therewith, wherein each internal buffer is associated with a crosspoint of one of said N input ports and one of said N output ports;

a scheduling controller capable of selecting a first one of a plurality of queued head-of-line (HOL) cells from said input queues to be transmitted to a first one of said NxN internal buffers according to a fair queuing algorithm in which each of said queued HOL cells is allocated a weight of R_{ij} and wherein said scheduling controller is further capable of selecting a first one of a plurality of HOL cells buffered in a second one of said NxN internal buffers to be transmitted to a first one of said output queues according to a fair queuing algorithm in which each of said

internally buffered HOL cells is allocated a weight of R_{ij}, wherein a group of K queues share a combined capacity of 1, and

$$\sum_{i=1}^{K} R_i \leq 1 ,$$

where R_i is the guaranteed bandwidth associated with queue i, wherein any queue being non-empty over a time interval T can be guaranteed a bandwidth of R_iT+E, where E is a constant.

2. The packet switch as set forth in Claim 1 wherein said NxN internal buffers are disposed within said switch fabric.

3. The packet switch as set forth in Claim 1 wherein at least some of said NxN internal buffers are disposed within said N input ports.

4. The packet switch as set forth in Claim 1 wherein at least some of said NxN internal buffers are disposed within said N output ports.

5. The packet switch as set forth in Claim 1 wherein said NxN internal buffers are configure within said N output ports such that each output port has a fast internal speed-up of N output buffer that is shared at least partially by cells from all input ports.

6. A communication network comprising a plurality of packet switches capable of transferring data in cells comprising fixed-size packets, wherein at least one of said packet switches comprises:

N input ports capable of receiving and storing cells in a plurality of input queues;

N output ports capable of receiving and storing cells from said N input ports in a plurality of output queues;

a switch fabric for transferring said cells from said N input ports to said N output ports, said switch fabric comprising an internally buffered crossbar having NxN internal buffers associated therewith, wherein each internal buffer is associated with a crosspoint of one of said N input ports and one of said N output ports;

a scheduling controller capable of selecting a first one of a plurality of queued head-of-line (HOL) cells from said input queues to be transmitted to a first one of said NxN internal buffers according to a fair queuing algorithm in which each of said queued HOL cells is allocated a weight of R_{ij} and wherein said scheduling controller is further capable of selecting a first one of a plurality of HOL cells buffered in a second one of said NxN internal buffers to be transmitted to a first one of said output

queues according to a fair queuing algorithm in which each of said internally buffered HOL cells is allocated a weight of R_{ij}, wherein a group of K queues share a combined capacity of 1, and

$$\sum_{i=1}^{K} R_i \leq 1 ,$$

where R_i is the guaranteed bandwidth associated with queue i, wherein any queue being non-empty over a time interval T can be guaranteed a bandwidth of R_iT+E, where E is a constant.

7. The communication network as set forth in Claim 6 wherein said NxN internal buffers are disposed within said switch fabric.

8. The communication network as set forth in Claim 6 wherein at least some of said NxN internal buffers are disposed within said N input ports.

9. The communication network as set forth in Claim 6 wherein at least some of said NxN internal buffers are disposed within said N output ports.

10. The communication network as set forth in Claim 6 wherein said NxN internal buffers are configure within said N output ports such that each output port has a fast internal speed-up of N output buffer that is shared at least partially by cells from all input ports.